

WHAT IS CLAIMED IS:

1. A semiconductor device formed by flip-chip bonding a semiconductor chip to a carrier used for external connection with the semiconductor chip, wherein:

the semiconductor chip includes:

5 a plurality of input/output cells including circuit elements formed so as to be peripherally arranged on a surface of the semiconductor chip, and

 a plurality of electrode pads formed on associated ones of the input/output cells;

 the electrode pads are configured in a zigzag pad arrangement so as to form inner
10 and outer pad arrays; and

 a predetermined area near a corner on the semiconductor chip surface is designated as a pad-disposition restriction area, within which disposing and usage of one or ones of the electrode pads that are bump-bonded to an interconnect pattern formed on a surface of the carrier are restricted.

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2. The device of Claim 1, wherein each of the electrode pads has a tenon-like conformation in plan view, and includes a narrow, probing portion for testing or analyzing, and a wide, bonding portion which is bump-bonded to the interconnect pattern on the carrier surface.

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3. The device of Claim 1, wherein the extent of the pad-disposition restriction area is determined in accordance with design rules for the carrier.

4. The device of Claim 1, wherein in the pad-disposition restriction area, part of the
25 inner pad array is not formed.

5. The device of Claim 4, wherein in the pad-disposition restriction area, a pitch for the outer pad array is reduced in accordance with minimum separation rules regarding disposition of the input/output cells.

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6. The device of Claim 1, wherein in the pad-disposition restriction area, neither the inner pad array nor the outer pad array is formed.

7. The device of Claim 6, wherein in the pad-disposition restriction area, instead of
10 some of the input/output cells which correspond to the inner and outer pad arrays, other types of function cells are disposed.

8. The device of Claim 1, wherein in the pad-disposition restriction area, the inner pad array includes probing-specific pads for testing or analyzing, and is not bump-bonded to
15 the interconnect pattern on the carrier surface.

9. The device of Claim 1, wherein in the pad-disposition restriction area, only one or ones of the electrode pads of the inner pad array are individually bump-bonded to the interconnect pattern on the carrier surface.

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10. The device of Claim 1, wherein in the pad-disposition restriction area, the inner pad array is individually bump-bonded to the interconnect pattern on the carrier surface, and at least two of the electrode pads are short-circuited to each other inside the carrier.

25 11. The device of Claim 10, wherein the electrode pads that are short-circuited to

each other inside the carrier are connected via the carrier to a power supply or to ground.

12. The device of Claim 10, wherein of the input/output cells, those corresponding to the electrode pads that are short-circuited to each other inside the carrier function as a single
5 high-drive-current capability cell.

13. The device of Claim 10, wherein of the input/output cells, those corresponding to the electrode pads that are short-circuited to each other inside the carrier function as a single low-impedance cell.

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